

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL' NUM 10076458	FILING DATE 02/19/2002	CLASS 324	SUBCLASS 501	GAU 2858	EXAMINER TURRESIN S.Y.
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**APPLICANTS: Tsuji Yoshio; Yamada Masayoshi;

**CONTINUING DATA VERIFIED: *None*

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-42356 02/19/2001

JAPAN 2001-111132 04/10/2001

JAPAN 2001-111133 04/10/2001

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed 35 USC 119 conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO 0052/064001
Verified and Acknowledged Examiner's initials <i>JT</i>		
TITLE : Circuit board testing apparatus and method for testing a circuit board		

U.S. DEPT. OF COMMERCE/PAT & TM-PTO-436L (Rev. 12-04)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWINGS	
Amount Due	Date Paid	Sheets Drawn	FIGS. Drawn
TERMINAL		Primary Examiner	
DISCLAIMER		Application Examiner	
PREPARED FOR ISSUE			
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